

**REMARKS**

This amendment is in response to the Office Action of March 19, 2001.

Claims 1 through 39 are currently pending in the application.

Claims 1, 7, 12 through 14, 20, 25 through 27, 33, 38, and 39 were rejected under 35 U.S.C. § 102(b) as being anticipated by Yoshigai (United States Patent 5,606,199).

Claims 2 through 6, 8 through 11, 15 through 19, 21 through 24, 28 through 32 and 34 through 37 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshigai (United States Patent 5,606,199) and further in combination with admitted prior art.

**35 U.S.C. § 102(b) Anticipation Rejections**

**Anticipation Rejection Based on United States Patent 5,606,199 to Yoshigai**

Claims 1, 7, 12 through 14, 20, 25 through 27, 33, 38, and 39 were rejected under 35 U.S.C. § 102(b) as being anticipated by United States Patent 5,606,199, issued to Yoshigai (hereinafter “the Yoshigai reference”). Applicant respectfully traverses this rejection.

Applicant submits that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The Yoshigai reference does not contain the detail that is contained in the presently amended claims.

The current application contains amended independent claims 1, 14 and 27 which all include the limitation that the paddle in the invention is attached to a side rail “by at least a plurality of paddle support bars and is further attached to a plurality of cross members by said support bars.” Further, amended independent claims 1, 14, and 27 all contain the limitation of at least one projection connected to at least one bond pad of said plurality of bond pads on the active surface of said semiconductor die directly connected to a substrate, the projections including one of at least one solder ball and at least one solder bump.

The Yoshigai reference teaches an island 7, with a central recess 7a as a chip support section in which the semiconductor chip 4 is mounted. The Yoshigai reference fails to include the frame which includes the side rails, cross members and paddle which is attached to the side rails by paddle support bars and to cross members by paddle support bars that is described in the present set of independent claims. Semiconductor chip 4 could be connected to a substrate such as a circuit board using LF leads 6.

Applicant submits that the Yoshigai reference fails to teach the limitation of amended independent claims 1, 14, and 27 at least one projection connected to at least one bond pad of said plurality of bond pads on the active surface of said semiconductor die directly connected to a substrate, the projections including one of at least one solder ball and solder bump. On the other hand, the Yoshigai reference teaches connecting LF leads 6 to the bond pads on semiconductor chip 4 by a thermal process or an eutectic process. The LF leads 6 could then be connected to a some type of circuit board.

Applicant respectfully disagrees with the Examiner's assessment that the Yoshigai reference teaches a paddle being attached to the side rail by a plurality of paddle support bars 3d and being attached to a plurality of cross members 3G by the support bars. Applicant asserts that 3d and 3G, shown in the Yoshigai reference, are ground and branch electrical leads that connect the electrode pads of a semiconductor chip to the lead frame. 3d and 3G are not structural members but serve to electrically connect the lead frame to a semiconductor. Even assuming 3d and 3G are structural members, the Yoshigai reference still fails to teach a generally centrally positioned paddle being attached to the side rail by at least a plurality of paddle support bars and being attached to said cross members by said support bars. The Yoshigai reference teaches the side rails, *if they are to be considered side rails*, are connected directly to the paddle and lack the above stated limitation.

Therefore, the Yoshigai reference fails to anticipate the present invention because it fails to teach every aspect of the independent claims of the present invention as required by *Verdegaal Brothers*. Because the Yoshigai reference fails to anticipate the presently claimed invention of

novel independent claims 1, 14, and 27, dependent claims 7, 12 through 13, 20, 25 through 26, 33, 38, and 39 are not anticipated. Further, dependent claims 12, 25, and 38 are not anticipated by the Yoshigai reference because it fails to teach an assembly including a substrate having circuit connections, with bond pads bonded to the circuit connections. Therefore, Applicant requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(b).

### **35 U.S.C. § 103(a) Obviousness Rejections**

#### **Obviousness Rejection Based on United States Patent 5,606,199 to Yoshigai in View of Applicant's Admitted Art**

Claims 2 through 6, 8 through 11, 15 through 19, 21 through 24, 28 through 32, and 34 through 37 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Yoshigai reference in view of the applicant's admitted prior art.

Applicant submits that the combination of these references does not teach or suggest the presently claimed invention.

The Office Action states that although the Yoshigai patent does not explicitly teach the product of claims 2 through 6, 8 through 11, 15 through 19, 21 through 24, 28 through 32, and 34 through 37, but that the Applicant's own application allegedly teaches that the product would be well known. Furthermore, the Office Action purports that it would have been obvious to combine the known products with the product of Yoshigai because it would facilitate connection of the die to the circuit substrate and the paddle.

Furthermore, Applicant submits that a *prima facie* case of obviousness has not established under 35 U.S.C. § 103. To establish a *prima facie* case of obviousness under 35 U.S.C. § 103, the following criteria must be met:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.**

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The present invention of dependent claims 2 through 4, 15 through 17, and 28 through 30 teaches projections enabling "gang" bonding, i.e. flip-chip bonding, of the semiconductor die bond pads to the conductive traces 46 of a substrate 42 such as a circuit board. There is no motivation or suggestion to combine Applicant's disclosure with the Yoshigai reference to arrive at the invention of dependent claims 2-4, 15-17, and 28-30. There is no motivation to modify the Yoshigai reference with the limitations of dependent claims 2 through 4, 15 through 17, and 28 through 30 because the active surface of the semiconductor in the Yoshigai reference is encapsulated and is incapable of being connected to a substrate in such a way. Only using hindsight is the Applicant's invention taught.

The present invention of dependent claims 5, 6, 8 through 11, 18 through 19, 21 through 24, 31, 32, and 34 through 37 are nonobvious as they depend on novel and nonobvious independent claims. Furthermore, dependent claims 5, 6, 18, 19, 31, and 32 all contain the limitation of using an electrically non-conductive adhesive layer to secure the semiconductor to the generally centrally positioned paddle. The Yoshigai reference teaches the opposite. The Yoshigai reference teaches "[t]he semiconductor chip 4 is mounted by *conductive* paste (not shown) or the like..." (Emphasis added, Column 4, Lines 53-54). It is improper to combine references where the references teach away from their combination. See MPEP 2145(X)(D)(2). Therefore, the rejection of dependent claims 5, 6, 18, 19, 31, and 32 cannot stand.

Therefore, the cited prior art fails to establish a *prima facie* case of obviousness for the present invention as in claims 2 through 6, 8 through 11, 15 through 19, 21 through 24, 28 through 32, and 34 through 37. Thus, the Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103 regarding claims 2 through 6, 8 through 11, 15 through 19, 21 through 24, 28 through 32, and 34 through 37 and the case be allowed for issuance.

Applicants submit that claims 1 through 39 are clearly allowable over the cited prior art.  
Applicants request the allowance of claims 1 through 39 and the case passed for issue.

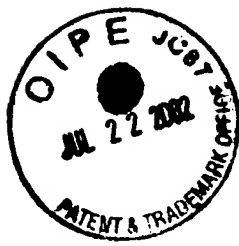
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**VERSION WITH MARKINGS SHOWING CHANGES**

**IN THE CLAIMS:**

1. (Three Times Amended) A semiconductor device assembly, comprising:  
a semiconductor die having an active surface having a plurality of bond pads thereon and an opposing second surface;  
at least one projection connected to at least one bond pad of said plurality of bond pads on the active surface of said semiconductor die [for direct connection] directly connected to a substrate, said at least one projection including one of at least one solder ball and at least one solder bump; and  
a generally centrally positioned paddle of a lead frame of a plurality of lead frames having side rails and cross members connected to said paddle, said second surface of said semiconductor die being secured to said paddle;  
and said generally centrally positioned paddle being attached to the side rail by at least a plurality of paddle support bars and being attached to said cross members by said support bars.

14. (Three Times Amended) A semiconductor device assembly, comprising:  
a semiconductor die having an active surface having at least one bond pad thereon and an opposing second surface;  
at least one projection secured to said at least one bond pad on said active surface of said semiconductor die [for direct connection] directly connected to a substrate, said at least one projection including one of at least one solder ball and at least one solder bump; and  
a metal paddle from a lead frame, said second surface of said semiconductor die being attached to said paddle; and  
said metal paddle is attached to at least one side rail by at least a plurality of paddle support bars and being attached to a plurality of cross members by said support bars.

27. (Three Times Amended) A semiconductor device assembly, comprising:

a semiconductor die having an active surface having a plurality of bond pads thereon and an opposing second surface;

a plurality of projections connected to said plurality of bond pads [for direct connection] directly connected to a host circuit board, said plurality of projections including one of a plurality of solder balls and a plurality of solder bumps; and

a metallic paddle secured to said second surface of said semiconductor die, said metallic paddle being attached to at least one side rail by at least a plurality of paddle support bars and being attached to a plurality of cross members by said support bars.